MSF REFERENCE Mark 2 by G4JNT

The Mark 1 MSF locked frequency reference was published in the April/May 1994 issues of RadCom. After several years of use a number of shortcomings have became apparent:

1) As published, the loop time constants are too short to ensure a really stable signal when the output is multiplied up to microwave frequencies. When listening to the CW note on 10 GHz the tone randomly wanders several hundred Hz over a few seconds; this is much worse at night where the shift can reach 1 kHz.

2) A 10 MHz output was needed to drive the reference inputs for a synthesiser and counter. The original version, since it had its VCXO at 12 MHz, could not produce 10 MHz without extra circuitry.

3) The gated signal approach using a tone decoder was a bit of a liability when signals became weak or QRM was present.

The first problem was initially overcome by increasing the value of the resistors R1 and R2 in the phase locked loop to 1M and 47k respectively. This gave a loop bandwidth of 0.02 Hz and resulted in a very significantly more stable signal, BUT meant a much more difficult start up procedure since the crystal oscillator had to be adjusted to within about 0.1 ppm before the loop could lock. A crystal heater was essential and the loop could still jump out of lock if the temperature changed rapidly, such as when caused by the sun suddenly shining on the unit. With a loop bandwidth this narrow, the sidebands caused by the signal pulsing on and off at 1 Hz rate will be filtered out and the need to gate the phase detector output into a sample and hold circuit is eliminated.

The requirement for a 10 MHz output overrode all else and so the Mk2 was constructed The same MSF receiver head as employed for the Mk1 was used, and the original article should be referred to for details.The circuit is shown in Figure 1 and consists of a 10 MHz VCXO followed by a divider to 1 MHz; buffered outputs at these frequencies are provided. The crystal is a high stability unit (10 ppm over 10 - 70 deg) available from several suppliers and so far a heater has not appeared to be necessary. A bandpass filter selects the third harmonic at 3 MHz which is amplified and divided by 50 to derive the 60 kHz reference signal. The phase detector is simplified over that shown in the original article by the use of a 4046 PLL device. This already contains an amplifier for the signal input, removing the need for a comparator at the MSF signal input port. To assist in initial lockup two switchable loop time constants were incorporated as well as a open position. The long time constant was chosen solely by what components were available. A non-polarised capacitor is necessary since it will have 0V across it most of the time and a 10uF was to hand. A 100M resistor is the highest reasonable practical value available giving a loop bandwidth of 0.02Hz. A blip filter is still required to completely remove the 1 Hz switching component however, but by making the cut-off frequency significantly higher than the loop bandwidth, its effect on loop stability is negligible.

Initially start with the loop open, the meter switched to indicate phase and adjust the oscillator trimmer capacitor for a frequency error of less than one cycle per 20 seconds as shown on the phase meter. This adjustment is made somewhat complicated by the meter reading fluctuating as the signal pulses on and off, but with a bit of practice the setting can be performed easily enough. Switch to short and the loop should lock up within two beats, shown by the meter settling to the centre of its range. This lockup time is minimised if the switch is moved as the meter indication passes its centre position whilst free running. After a few minutes of stable operation, switch to long, sit back and have a long wait (or better, forget it for a few

hours). The meter should not move more than a tiny fraction but the loop is still minutely stabilising. This can be seen if another very stable and accurate source of 10 MHz is available by comparing the two signals on a scope. Switch the meter to indicate control voltage and observe over several days. The reading will change as temperature varies, but if a high stability crystal (such as Farnell part No. 103-887) is used this should only be by a percent or so. The long winded setting up procedure is not something to be repeated many times, so the unit should be left running; the provision of battery back up would be advisable especially if power cuts are a common occurrence!

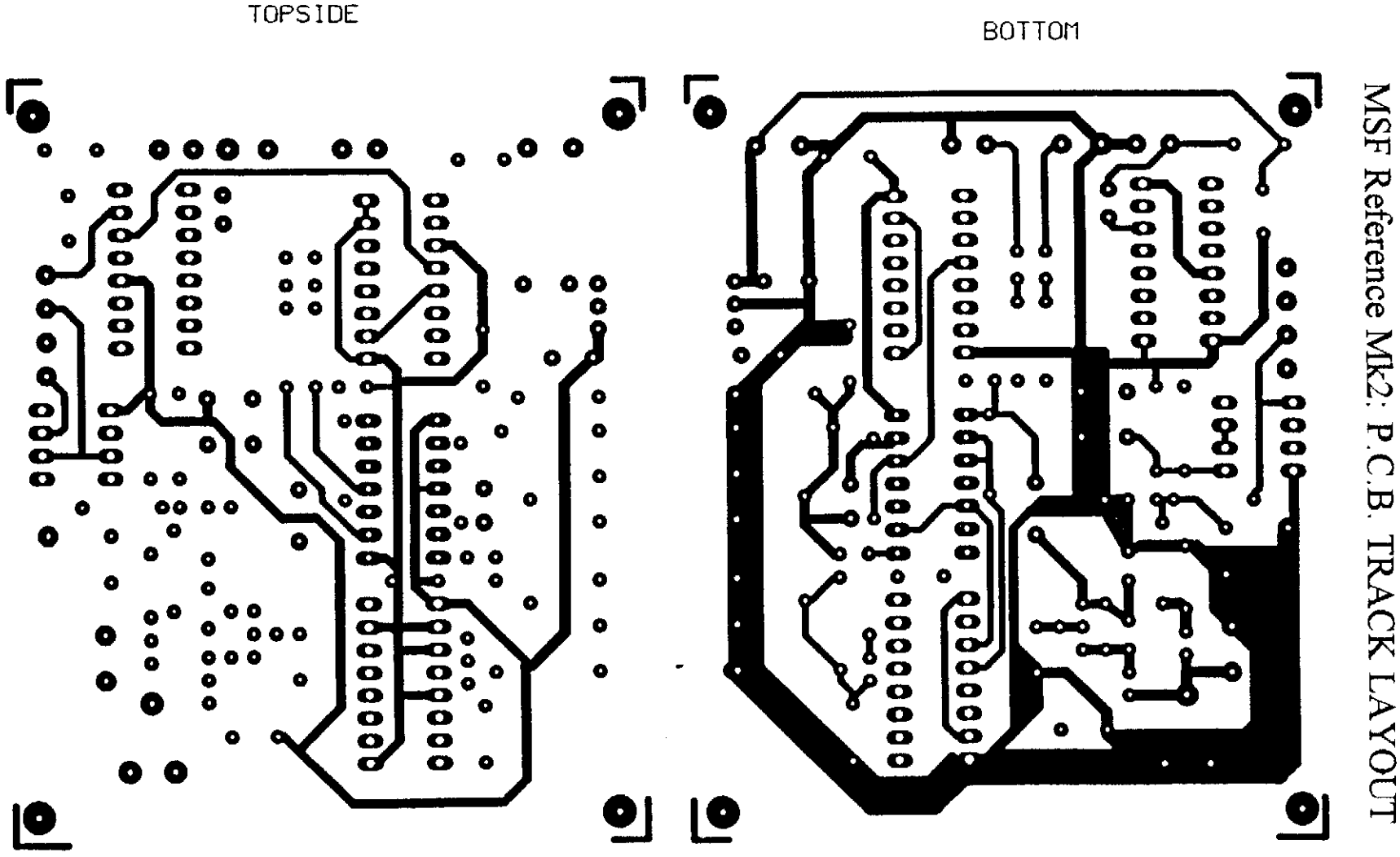
Long term comparisons over several days have been made against known very stable signals such as from Rubidium and Caesium sources, and a short term stability (short term means tens of minutes here) of 2 parts in 109 is regularly achieved (this is 20 Hz at 10 GHz). These variations are caused primarily by random perturbations on the MSF signal causing the loop to correct at its natural response, and so the short term stability is directly related to the loop bandwidth and damping. If this could be lengthened by a factor of 10, the stability would improve by the same amount - owever we are now talking about a C.R1 product of 3 hours, a crystal oven would be essential so perhaps everything should be done digitally using DSP techniques.

The 10 MHz output is not perfectly buffered and connecting a load here once the loop has stabilised results in perturbations which take about 10 - 20 minutes to die away

To aid experimentation, a table of values for C.R1 and C.R2 product is given for differing values of loop bandwidth. These assume that the VCXO is built exactly as shown, with the crystal type as given, resulting in a frequency / voltage variation of around 60 Hz / volt at 10 MHz (Kv =3D 0.36 Hz/V when referred to 60 kHz). A cheaper / lower stability crystal may result in a greater Kv value, meaning that the T1 and T2 values need to be re-calculated for an optimum loop response.

A double sided PCB has been designed, with the loop Rs and Cs off board to aid experimentation; contact me direct for the layout, but there is no intention of making finished PCBs available.

Loop Bandwidth (Hz)	C.R1 (seconds)	C.R2	
0.3	2.9	1.2	
0.05	138	8.7	
0.1	32	4.2	Short
0.019	1000	23	Long
0.01	3600	45	
0.005	14600	96	



MSF Reference Mk2: P.C.B. TRACK LAYOUT

ERRATA: The 10n capacitor shown in the circuit diagram connected to pin 13 of U1F (74HC04) is missing from the track layout but can easily be accommodated by careful cutting of the foil near the pin.

MSF Reference Mk2: COMPONENT PLACEMENT

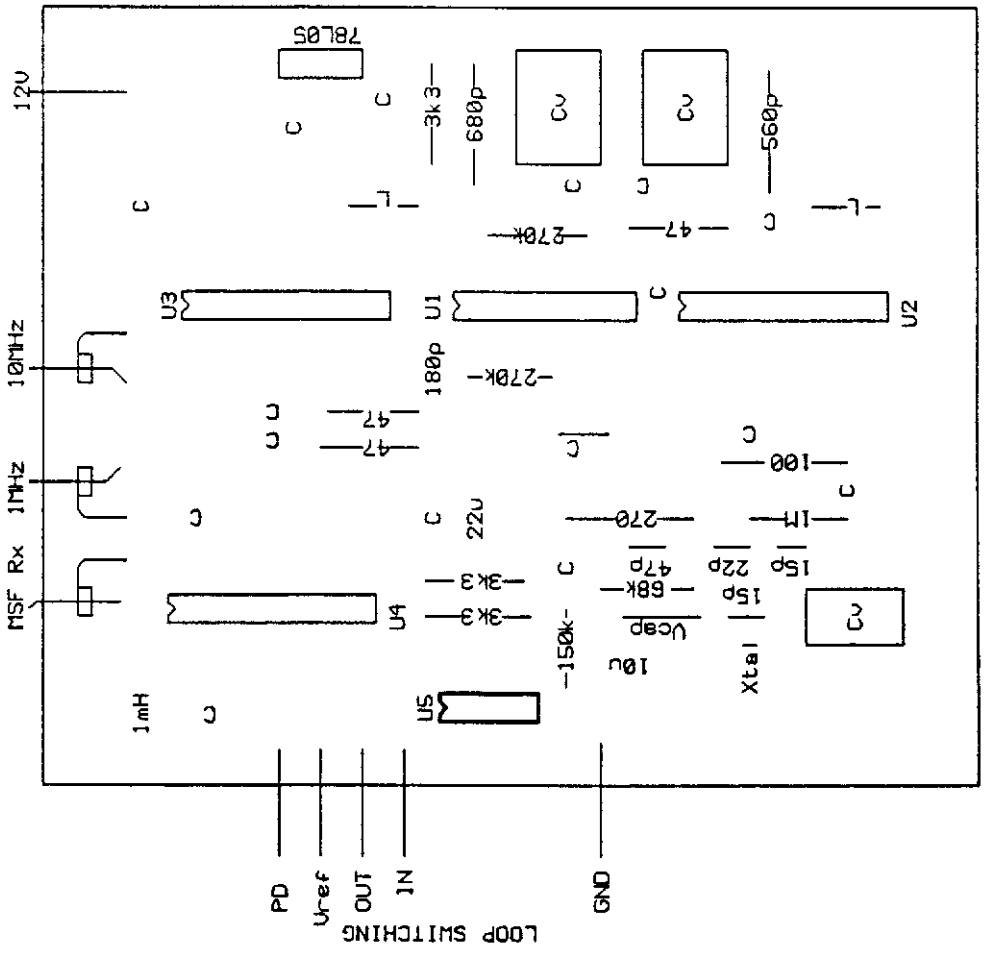
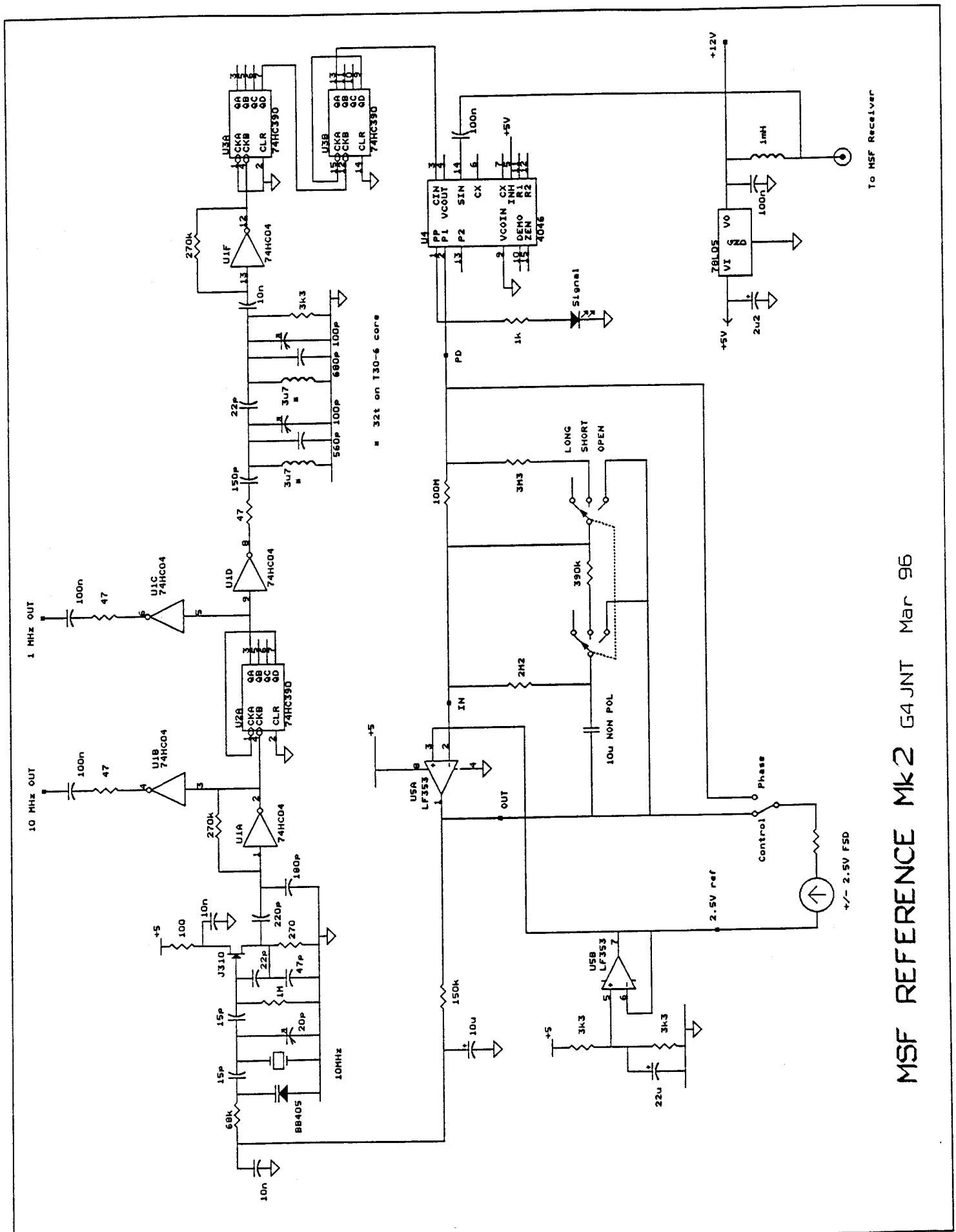


Figure 1:


MSF REFERENCE Mk2 G4JNT Mar 96
1 MHz OUT
10 MHz OUT
10MHz
* 32t on T30-6 core
LONG
SHORT
OPEN
Phase
Control
2.5V ref
+/- 2.5V FSD
To MSF Receiver
Signal
74HC04
74HC390
LF353
J310
BB405
78L05
4046