Conjugate Match Series

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Here is my conjugate match series from beginning to end written as a development piece taking what is generally known and building on that to the more particular requirements at RF. This was written in response to what was a raging controversy at the time about the topic which ran from 1995-ish to 2005-ish and spawned several articles both pro and con. The series takes the con viewpoint and develops that slowly by introducing solid-state techniques and notation then circling back around highlighting what is different and what isn't. The focus is to make completely general statements about the behavior of three-terminal devices whether they be BJT, FET, or Tube. I have kept the dialogue that shows the initial origins of how this started and I do have permission from the original recipients to re-use the material which is otherwise unpublished. Although math is invoked, it is described more than used for calculations.

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Introduction

I have been thinking a lot about this recently. I think it is time to review what is and was known from the best practitioners of tube design and characterization and then bring in my central theme. This is mainly that there is confusion on two levels:

1. There is definite confusion about having the device take power at the input and make power at the output. One can very nicely have one without the other. But there is no requirement that the output provide anything approaching a "conjugate" match to the load. This becomes apparent the further the device is driven away from Class A conditions. Although the term load line still means something in these cases, it becomes a very nebulous thing as the device must run over an optimized trajectory of voltage and current.
2. It is unfortunate that in tubes, the strays are of such magnitudes that they require resonating out while at the same time, at sufficient frequencies, are of the same order of magnitudes as the load line time-averaged impedance from the load voltage and current trajectories.
3. In solid-state designs, there is generally no confusion as the load line design criteria and actually operating the device in "matched" conditions as a voltage amplifier are likely far apart.

I need to refer to my 1994 paper from the VHF Conference about all classes of PAs and show their trajectories for both voltage and current in all of the different classes. These are true regardless of device type.

Part 1

Let's begin at the beginning at audio and low radio frequencies.....

Resistive loads--*BANG*! There goes the first balloon.....AF amplifiers although characterized for resistive loads rarely ever see one. The speaker load reflected through the transformer if any is reactive and broadens the load line into an ellipse. Thus, the amplifier plate voltage and plate current do not operate along a line but along a "trajectory". The trajectory becomes quite dynamic in the case of class B as one tube is completely cut-off while the other conducts. Think about what happens to the plate voltage of the cut-off tube.....

Input characteristics--Tubes and FETs operate at low frequencies as voltage probes with a slight capacitive component. The model is Ip=Vgk * gm where Vgk is determined across Cgk. There is no shunt resistive component in a tube or a FET at low frequency. This is strictly a function of the Miller effect caused by feedback through Cgp. A tube or FET (including MOSFETs) operates this way well into the RF range if gain is limited by swamping or other means. Thus, there is no way to get a tube or FET to take "power" in class A amplifiers at low frequencies and the input VSWR is infinite or determined by other components. It is quite possible to still have power amplification but no significant input power AT THE TUBE. We are discussing voltage swings only. Until the contribution fed back through Cgp or Cgp || Cgk forms a voltage divider or whatever, this is the situation. All HF power MOSFETs are exactly the same EXCEPT input capacitance is far higher so a very small amount of power is needed to charge Cgs or Cgd etc. This small amount of power is negligible compared to the amount lost in the swamping resistors and any stabilizing feedback.

Maximum Stable gain--Once the device becomes unstable, max. gain is no longer attainable but some amount of gain may be given the input/output Z s presented to the device. These may have to be evaluated in the bands of interest and outside. All devices have a -6 dB/octave roll-off at any frequency so gain is asymptotic at low frequencies. Provided the signal source is a high enough Z, large amounts of gain can be obtained until Cgd or Cgs and/or Cgp or Cgd can become a limiting factor. One way of dealing with this is to use a cascode circuit or active load as the IC designer's like to call it. Low frequency gains of 40-50 dB or more are easily attained with this circuit-even with 12AX7s!!

RF Amplifiers, Overdrive, and Class A--RF amplifiers can be treated as ideal txfmr coupled amplifiers for purposes of design. Note that push-pull or push-push designs are tractable at RF due to the flywheel effects of the tuned circuits smoothing out the plate current pulses in class AB, B, or C. An RF amplifier can be overdriven beyond the

compression point yielding increasing plate/drain efficiency or DC conversion efficiency. This is particularly true in class B, C designs where linearity is not a concern. Class B,C amplifiers are biased as shown in my paper with a comparatively steeper load-line impedance and the grid at cut-off or beyond. Note that Vp or Vd can exceed 2 Vpp (or Vbb if you like) during cut-ff conditions with no current other than the charging/discharging of Cgd and Cpk and that this instantaneous voltage follows a trajectory along the X-axis of a typical Ip vs. Vp graph with Vg as a parameter. i.e. , away from class A, Vp can run away to 2 Vpp in a transformer or tuned circuit on the cut-off tube or both if push-push. A class A transformer coupled amp. can have an efficiency approaching 50% IF overdriven with a square/rectangular wave voltage drive at the grid. This is a proof I remember doing in EE. However, the theoretical efficiency of a class B or C amplifier cannot increase in this way as the 2 Vpp swing is already accounted for at maximum output.
Note that the usual class A efficiency limit of 25% ASSUMES a resistive load....Check your textbook.

My paper is in the 1994 NE VHF conference collection. The drawings are lousy and there might be an error or two but the viewpoint may be useful. I am trying to generalize for all kinds of devices and breaking the amp up into simplified considerations regardless of frequency.

Last bit--The goal of designing a power amp is then to attain Vp max. simultaneously with Ip max. without burning the device up due to over-dissipation. i.e. the design must be for best possible efficiency and then add additional constraints such as linearity or gain from that point. It was known that the efficiency for a given bias condition was optimized for an optimum load resistance under low frequency AC conditions. The load impedance optimum was heavily influenced by the Vp and Ip conditions set by the plate supply and the grid bias. This same process is used to design switching supplies today where the actual phases of Vd and Id are manipulated by feedback or networks to have the desired waveforms so that device dissipation is minimized. This load-line impedance became the stepping stone for RF power design attempts. Some of the difficulties encountered are due to stretching this concept beyond all validity at RF.

I can get to other questions with more development. In the meantime, think about what we actually wish a PA to do.....CMG

********** wrote:

> I would say, "jump in", but to be quite candid, I don't follow you.

In addition, I have been away from this whole controversy for a while -- ever since receiving some private correspondence from Warren Breune that I can't find. (just went looking for it).

> First of all, I am assuming you are talking about amplifiers. If you are, how can you have an output without and input? With no input what are you amplifying?

> Just how do we match the load if not conjugately, which I take to mean the R+j of a different sign.

> How do you match anything of disparate impedances?

> Are we talking about a network or not? How does one effect a transformation without a network?

> What's a "stray" and what's a "sufficient frequency" and whats a "trajectory"? These terms mean nothing to me.

> I would like to see your 1994 paper. Maybe that would explain to me what you are talking about.

Part 2

Let's Review:

1. Load-line calculated as combined plate load projected from max. current point at minimal plate voltage to min. current point at max. plate voltage. (or drain or collector, etc.)

2. This calculation is only valid for Class-A and becomes increasingly inaccurate for Class AB1, AB2, B, and C.

3. In the more non-linear classes the load-line is not a line but a piecewise linear approximation with two slopes-one represents the device in cut-off and one represents the device in the active region. In Class B, the approximate lengths of these two line segments are equal. In Class C, the two segments are very unequal-the plate swings much further in cut-off than when active.

4. The Load-line thus calculated for classes departing from Class A is an approximation at best but much greater insight can be had looking at the actual trajectories of the plate current and voltage swing.

5. A Class-A amplifier operating with a tuned load can have efficiencies close to 50% with the correct grid drive. An RF amplifier may be analyzed as if an ideal

transformer was coupled to its load and the current generator (ip=gm * Vgk) over a narrow bandwidth.

6. A reactance reflected back into the amplifier output stage broadens the Load-line into an ellipse which in the case of greater non-linearities can be piecewise continuous.

7. A Class A amplifier cannot take power from the driver at low frequencies. The grid is a voltage (capacitive) probe. A Class B amplifier or a Class AB2 does take definite power as the grid conducts over some portion of the cycle. Modern MOSFET amplifiers are designed without much thought given to the capacitive parasitics by using feedback and swamping techniques.

8. Tubes do not exhibit grid loading until very high frequencies where transit time or Miller Effect become appreciable. Tubes can be operated up to their Maximum Stable gain or even the Max. Available gain provided Cgd is small or insignificant compared to grid loading. This is true for FETs as well. All circuits accumulate gain at +6 dB/octave as frequency decreases.

9. Active loads (cascodes) are very effective means of minimizing Cgd to obtain high gain and low noise.

10. Audio amplifiers are designed into resistive loads but loudspeakers are anything but. One reference I consulted said impedances 10 x greater than designed are quite often measured. I don't think there were corresponding suck-outs where Z load << Z designed though it could occur. So even the low frequency case has holes in the Load-line design process. Much more insight is to be gained through simulation of the voltage and current swings within the device.

Now, to continue:

Practical tubes and FETs as well as BJTs have finite resistance or leakage. Transistors and FETs also have reverse leakages that are modeled with weakly conducting non-ideal diodes in most simulation programs. The family of curves generated by steps in gate or grid voltage or base current has a slope which is 1/R denoted as Rp or Rce or Rds for DC values. Devices such as tetrodes and pentodes as well as most bipolars feature very high values of R (more and more like ideal current sources). Triodes have a much lower DC R value and there is sufficient loading that this value must be taken into account as part of the overall plate load (Rp||Rl'). Note that this is a resistive term (actually a conductance) and DISSIPATES Power!

At AC, all devices show some greater conductance of the current/voltage steps from the input drive function than at DC. this can be verified by pulse testing of the device dynamic characteristics to avoid thermal effects. This conductance is r and is written rce,

rp, or rds following the convention of AC values using small letters. This is also a resistive term and DISSIPATES Power.

Any device on God's green earth then has an AC resistance at the plate/collector/drain of rp/rce/rds. There is also a Rp/Rce/Rds term in parallel with it that may or may not be significant. The current generator of the device is said to be shunted by these terms and at low frequencies forms the output Zout of the device assuming there is no feedback. Thus, the conjugate match of any device is to this Zout for max. gain! You will not do better than this and it can't be resonated out or absorbed. Fortunately, it is usually small enough to live with EXCEPT in the case of really BIG TUBES where Zout ~= the desired Load-line!!!! Fortunately, this is still not a problem as long as Max. gain is not desired but IT IS a drag on efficiency.

Amplifier designers have long defined efficiency as Pout/PDCin. No surprises there. However, an amplifier can be driven well past theoretical limits to increase efficiency beyond the limits of the class of operation. The microwave industry coined "power-added efficiency" defined as Po/(Pdc + Prfin)to get around these designs. So an overdriven amplifier may have higher DC efficiency but the PAE is heading downhill as more drive power is required. Most all devices have theoretical peak PAE around the P-1 dB point, that is, when the driver power must be increased by 1 dB to maintain output above what it was before or when the insertion gain has decreased by 1 dB (the best definition).

Now we're getting somewhere. It has been shown that the Rp/Rce/Rds and rp/rce/rds components of the plate/collector/drain resistance are both statically and dynamically resistive and that they dissipate POWER. This alone contradicts some of the experts writing in the mags.....*But wait! There's more!!* At low frequencies, the Zout of the device is just this R xx || r xx shunting the current source and the (so far) insignificant Cpk/Cce/Cds output capacitance.

If I wish to design the amplifier for Max. gain-no matter what class-I design the output load to look like R xx! This may or may not correspond with the point of operation desired for max. efficiency or power output. Note that max. power output MAY NOT occur at the max. efficiency point but should be close. Further constraints on IMD performance etc. make this more of a compromise. A solid-state device, for example, has regions of breakdowns particularly at RF where it is wise to stay out of so these may be constrained yet again.

Let's think about what a PA has to do....We want to operate the device in the region where max. voltage swings and max. current swings occur in phase or reasonably close to it. We can use the flywheel effect of the tuned circuit to carry us over the hump when the amplifiers depart from Class A so when the tube is cut-off, the output swing can be even higher due to resonance of the tuned circuits. Here is where knowledge of the trajectories of the voltage and current pay-off well. If we know what the voltage and currents are doing instantaneously over time, the driving waveform and output Z load can be tailored to obtain the desired results. This is how Class E RF PAs were invented-by carefully

analyzing the overdriven case where the amplifier is pushed well beyond initial compression. We want to prevent the device from burning up so efficiency at the device is still important.

[**Aside**] There has been considerable effort in commercial circles at fixed bands to use impedance tailoring and harmonic tuning as noted above in amplifier designs. Both input and output tuning consisting of shorts and opens to even and odd harmonics have been used at the cellular/PCS/Wi-Fi frequencies to very good effect. The tuning scheme used defines the sub-class of operation E, F, G, H, and so on. Since hams also have fixed frequency bands, are we not missing the boat?

Conventional amplifier design using Load-line techniques uses well-worn rules-of-thumb to approximate the desired Load-line resistance. Accommodation is then made for the reactive elements in the network designs to absorb C xx at the output of the device. These approximations are:

Class A: Tube Vbb/(k * 2Po) ; where k=1.0 to 1.3 usually 1.2

Class B: Tube Vbb/(k * 2Po) ; where k=1.5 or pi/2

Class C: Tube Vbb/(k * 2Po) ; where k=2 or greater (in a multiplier stage?)

Class A: Transistor (Vcc-Vcesat)**2/2Po ; where Vcesat ~= 0.2 V

Class A: FET/MOSFET (VDD-IdssatRdssat)**2/2Po ; where Ids sat is Ids, Max. and Rds sat is Rds minimum.

Class B: SS (Vxx-Vsat)**2/pi * 2Po [**1**]

What all of these formulae are really doing is allowing for the region where the device has no gm (transconductance) right around 0 Vxx.

In BJTs, this curve is sharply defined whereas in FETs it is mushy and depends on the FET but is typically around a volt. Within tubes, the breakpoint can be much greater on the order of 10s of volts or even 100s of volts for BIG tubes. The region discussed here is where no amplification takes place but the device is drawing current so it must be accounted for in power estimates.

The above relationships are useful at low frequencies for solid-state or vacuum tube design. Although the equations look different, I would maintain they are fundamentally the same but no one looked for a close form of Vpk sat in a vacuum tube before the tube era engineering efforts closed. If such an expression were to be derived, then the solid-state formulae should be capable of being used once Vpk sat (to use modern SS notation for once) is determined.

Now, it is time to enter the world of real radio frequencies where transit time and inter-electrode capacitances play. The fundamental effects of transit time is to increase the grid admittance [**2**] so that it effectively shunts the input circuits thus requiring drive power to maintain the same plate swing at higher frequencies. This is called the "Miller" admittance and is directly proportional to frequency. At the same time, Cgp/Ccb/Cdg is now presumed large enough to couple significant output energy to the input. Miller's theorem states that this effect can be thought of as two capacitors one shunted across the input which is Cyy * Av and the other is Cyy/Av shunted across the output. (I am ignoring a +1 term for this as not relevant.)

So the contribution to the output circuit || C xx is favorable but now the input is harder to tune, match, and, by the way, it now takes power. But there is a loophole, the partitioning of the capacitance is dependent on Av only not Ai or any other parameter so in circuits where Av is reduced at the input stage such as the cascode, or the grounded grid, the problem is lessened. The grid/base/gate admittance we can do little about except to note that owing to the small dimensions of SS devices, the problem is much less worrisome at HF but reappears at VHF and UHF. The input load is now an RC consisting of

((Cyy * Av)+ Cin + Cyy) || R miller at the tube pins.

The output load is now ((Cyy/Av) + Cxx) || Rxx || R load.

The HF/VHF form of our device input and output Zin and Zout have now been determined to a first order to be an RC parallel circuit. (think admittances!) The output RC shunts the current generator while the input RC shunts the capacitive grid probe upon which the signal voltage is developed Cgk/Cbe/Cgs. The max. gain obtainable from the device is still now tuned somewhat inductive at the INPUTS PRESENTED to our device matched to R xx at the output and Cyy + (Cyy * Av) + Cin || R miller at the input.

So we have already deviated from a true conjugate match in order to tune out the bothersome capacitances. In practice, these are resonated or absorbed by a choke coil in a shunt fed system or a small series matching inductance or even some lead or track inductance on a PCB for the frequency of interest. Note that broadband operation cannot be obtained this way but there are still circuit design tricks left in the black book.

It is instructive to consider the Load-line effects of the typical parameters in a solid-state design and a vacuum tube design. This is why I think there is so much confusion, For most SS design activity, the load-line as determined by the equations given is NOWHERE near the values of R xx || C xx needed for max. gain. In the vacuum tube case, it often may be LOWER than the Load-line desired by a LOT. Thus, a tube circuit must spend more tank circuit "**Ql**" to absorb these reactive components and thereby decrease efficiency. There's a reason why those VHF glass-to-metal or ceramic-to-metal seals get HOT. The circulating currents and the resulting real power in the tuned circuits to absorb the reactances are immense. Also why low inductance and low resistance contacts are needed in high power VHF tubes which drives one into a cavity or T-line design. Owing to the very low impedances typically used in a solid-state design at the device level, very high circulating currents again exist right at the device input and output

terminals so both amplifiers sort of have this similar physical realization problem but they ARE DUE TO DIFFERENT CAUSES!!!

The ideal RF coupled transformer used earlier to avoid discussing matching networks to early may be replaced by a T-line at the frequency of interest. However, reactance does not reflect back in a T-line the same as in an ideal transformer although for an ideal ¼ λ lossless line resistance does. Losses in the T-line are even more problematic for getting the correct reactance to reflect back at the input. Use substitutions such as this with a great deal of caution.

Part 3

Let's Review Part 2:

1. Introduced the idea of finite static and dynamic plate/collector/drain conductances as evident from inspection of characteristic curves on the devices.

2. Developed the low-frequency forms of equivalent output circuits using the conductances mentioned above and output-to-RF Ground shunt capacitance. The requirements for "matching" the resulting circuits were briefly touched upon here.

3. Criteria of max. gain or max. stable/available gain was used to discuss the "requirements" of matching to the device.

4. Approximations (mainly from the 1994 ARRL Handbook and others) were introduced to calculate the resistive optimum load impedance for both tube and solid-state amplifiers. The necessary approximations were also discussed in some detail.

5. Efficiency in regard to power amplifier design was introduced along with revisiting the concept of overdriven amplifiers. Power-added-efficiency was discussed in light of the above with the need to account for driving power.

6. My own speculation about the utility of harmonic tuning methods for amateur usage was inserted into the text at this point. These methods have been very fruitful in the commercial world and have been optimized for modulation types leading to the modern highly efficient portable cellular phone transmitters.

7. The real world at HF and VHF (for tubes) and VHF and microwave (for SS) was introduced in all of its relative ugliness wit the added inter electrode capacitances for both the input and output equivalent circuits of the device. The form of the native equivalent circuits is shown to be primarily parallel RC.

8. Real world effects of transit time leading to grid shunting conductance, instability, and reduced gain were discussed. The input-output coupling capacitance Cgp/Ccb/Cdg was shown to have a large effect on the input equivalent circuit IF the device had a relatively high voltage gain. If the output swing was constrained (current mode) operation, then the effects could be reduced. Effects on the output equivalent circuit were found to be almost negligible.

9. The full frequency behavior of the device can now be written by inspection up to the next series of significant effects from increasing frequency. The parallel RC description adopted here will suffice for the remainder of the text.

10. Both SS and thermionic devices were shown to have significant circulating currents due to reactive elements in their tank and input circuits. In the case of the SS amplifier, the circulating currents are due to the very low optimum load impedance required to extract power from the device while in the tube case, the currents are mainly parasitic as they are BELOW the desired optimum load line impedance and so must be parallel resonated over narrow bands. Note that the SS parasitic inter electrode capacitances generally have resultant reactances well above the optimum load particularly at the output.

It is now necessary to develop some further conventions of HF/VHF/microwave measurement parlance; to introduce the idea of reflection coefficients and S-parameters which will then naturally lead into the discussion of what is a conjugate match criterion. Any two-port device may be described by a set of four parameters in such a way as to uniquely specify its small-signal performance over frequency with an array or at a single frequency at a time. This is the usage which will be intended here. Four parameters serve to specify the input and output matching or lack thereof, gain, and isolation or Reverse gain if you prefer.

S-parameters can be conceptualized as launching waves into a generalized "thing" at input and output and observing the response for both reflections at the ports and any transmission or attenuation. All of the quantities involved are vectors so both a magnitude and phase angle are assumed. These may be resolved into G-jB form on a Smith chart or converted to R+jX form using the same chart.

S11 Input Refl. Coeff. b1/a1

S12 Reverse Transmission (isolation) b1/a2

S21 Forward Transmission (gain) b2/a1

S22 Output Refl. Coeff. b2/a2

The "b" reflected and "a" incident components specify the directions and ratios used to form the S-parameters for ports 1 and 2 of the two-port device. An "a" wave is defined as going "into" the thing from either direction whereas a "b" wave is defined as coming "out

of" the thing. These considerations and the extension to multi-port devices allow any conceivable device to be tested using similar notation and similar test equipment. The S-parameters may be expressed in either scalar or logarithmic form but the waves are considered to be defined as a voltage to/from a source. One may not use power as a basis of S-parameters since without the knowledge of phase before the measurement, power is not clearly defined. S-parameters may be taken at spot frequencies or swept over an entire band or more to characterize the device. The other consideration is that they are only valid under small-signal conditions; i.e. when the device is still linear. Though there have been attempts to use S-parameters in non-linear design by Motorola among others, these represent proprietary techniques and knowledge as well as equipment not generally available to the amateur.

If S-parameters are not valid for large-signal characterization such as PAs-what does work? Suppose by dint of being good looking and smooth talking, I seduce the manufacturer into giving me a brand new device, heretofore unheard of by science, and wish to characterize it or build an amplifier around it. Let's call the device the "SWETFET". Well, I have to know a few things about it so let's say I have a little knowledge of the DC characteristics and don't blow up too many while getting that data. I then construct a test fixture with ports on it that allow me to apply variable impedance loads such as RLC parallel or series circuits, transmission lines with sliding shorts, or microwave double-stub tuners. I then vary the tuner mechanism until I obtain output at a given frequency or white smoke. Once I obtain the output, I shut down the SWETFET, carefully walk over to the Vector Network Analyzer (VNA) and measure the S-parameters of the tuned circuit which are perfectly valid for passive circuits. I then repeat this process with the input while trying to maximize my output power and then go back and retouch the output adjustments etc. Microwave guys call this procedure a "Load Pull" [**3**] If I was trying to do a low-noise amplifier, the output would be tuned last and the input would be tuned first with an input of broadband noise rather than a driving signal applied. This is then referred to as a "Source Pull". If all of my measurements are correct, I end up with regions of input and output contours on the Smith chart that correspond to maximum output power. Such a chart can be referred to as a Rieke diagram for that device if designing for output power and a noise contour plot if designing for low noise.

One possible design procedure now referred to as the Cripps method but formerly known as close your eyes and pray is to design the output circuit for the conjugate of the contour identified for the output circuit during the load pull while designing the input circuit for either the identified input circuit contour conjugate or the small-signal parameters obtained at the desired bias-assuming the device was stable. The designer's job is to insure that the impedances fall on the contour's conjugate by tailoring the reactances and networks to do the matching task while ultimately driving the desired output impedance.

The only thing that we are concerned about here is getting the "conjugate of the output contour" presented to the output of the SWETFET and the "conjugate of the input contour" presented to the input of the SWETFET. Curiously, the approach works pretty well and can be within about 10% of the final optimal values if the utmost care and

precision is used. Other methods of design using SPICE models or hybrid time and frequency domain models exist for computer simulation and design. Weakly conducting anti-parallel diodes or controlled voltage or current source pairs are often used to mimic real world physical effects due to substrate back gating effects, leakages, breakdowns, etc. Note that no effort was made to obtain maximum voltage gain from the device - This is a hint!

How was the end impedance of the terminating matching networks in either case determined? By connecting it to the desired terminating impedance at the input/output terminals-most likely 50 Ohms. That's right, as in all network synthesis, we decided what we wanted to have and what we needed and worked backwards! When the network is terminated in 50 Ohms at the far ends, it presents, at least in the band of interest, the desired conjugates of the contours determined by the Load Pull method.

How is the conjugate match defined as it has been discussed in the literature? By provision of a matching network such that the output reflection coefficient of the device and its matching network is zero. Ideally, we desire that the input reflection coefficient between the device and its input matching network also be zero but this is not required. BUT, the only time that this is true is for the input and output to be matched by parallel RL circuits to match the parallel RC circuits of the form discussed in Part 2. This arrangement is certainly convenient for bias feeding at the cold side of the coil. Thus unless the optimum load line happens to coincide with the exact values predicted by the small-signal work done earlier which generated the RC parallel circuit equivalents at the input of the device, the conjugate match condition DOES NOT and CANNOT exist!!!!!

We reiterate that the conjugate match can only be said to exist when the RC parallel circuits previously determined for the device are presented by networks that transform the desired terminating impedance to the conjugate RL forms of the equivalent circuits. In a power amplifier, the desired terminating impedance results in the conjugate of the device contours determined from the Rieke diagram. The only way that a conjugate match can exist is for, as stated previously, the RL parallel circuit equivalents to match those of the device resulting in NO reflections and therefore a perfect VSWR at the corresponding ports.

The contours determined by the load pull procedure may or may not reflect this. What they do reflect is that for a given bias condition, maximum power output was obtained for a certain conjugate input and output impedance presented to the device. If these sets of contours are not equal, then NO CONJUGATE MATCH may exist except at extreme overdrive or under drive conditions where the contours may coincide. If the output matching network is terminated at its desired impedance and the network alone is analyzed with the VNA, it will be shown to present the RL conjugate admittance within the band of interest AND when presented with the conjugate of that admittance in parallel, to have no reflections at the terminated end.

It is not possible to design for maximum gain and obtain a good match to the terminating impedance desired since maximum gain and therefore the conjugate match and maximum

power output do not occur with the same set of contours. It is possible to design with maximum gain at the input and to maximum power match the output for high linearity applications, but this is in general seldom done. The improvement in IMD though makes the procedure worthwhile. There exist techniques in the low noise case for modifying the Source Pull coefficients obtained to more closely match the parallel RC components of the device by means of feedback. Such readily available methods do not exist for power amplifiers, however as feedback depends on linear small-signal operation to be valid. Envelope feedback in the form of ALC is perfectly valid for use with PAs, of course.

All of the above considerations pertain to one unique set of bias conditions, frequency, and drive level. If any of these are to change significantly-say ± 1.0% or less in the case of high-Ql matching circuits, the parameters must be recalculated and new matching networks must be designed. A power amplifier is designed for maximum output power over a band of frequencies typically for one matching condition and at an expected efficiency. As drive power decreases, the efficiency falls off quickly while the load impedance increases toward the small-signal case limit. Thus, a power amplifier under conditions of low drive has poor efficiency with a load line impedance generally much higher than the optimal efficiency case at maximum power output. It can be shown that a Class B amplifier has an efficiency that falls off as 1/Pdrive**1/2 while at 6 db down, the load impedance is twice what it was at optimum. The design of any linear amplifier that is not constant envelope (FM, PM, QPSK) is a compromise between efficiency over all excitation conditions and ultimate power output. Constant envelope amplifiers may make use of such techniques as switched supply biases to optimize efficiency for a given drive level.

At low frequencies up to mid-VHF, absent internal device feedback, it is possible to talk about power matching the device where the impedance presented to the device is the conjugate of the optimal load impedance, and, gain matching the device whereby maximum gain is obtained and the input and output reflection coefficients presented to the desired input and output terminations are zero. It is not possible to do both in most cases. In either low noise design or power amp design, the gain obtained is a secondary or leftover parameter once the desired primary specification has been reached. Manufacturer's usually use the term associated gain when reporting these figures. It is also possible to use reflections back through the non-zero Reverse transmission of the device (S12) to "pull" the input as a form of feedback.

Part 4

Let's Review Part 3:

1. S-parameter notation was introduced, defined, and discussed with reference to its application to the particular problem of power amplifier design.

2. Introduced Load-Pull and Source-Pull procedures for determining optimum device load and source impedances for either max. power output, max. efficiency, best linearity, or least noise.

3. A hypothetical new device was used to illustrate a possible characterization effort that would be made in a semiconductor lab.

4. Descriptions of various design approaches including Cripps' method were included here as a means of discussing the general circuit design problem.

5. Relationships between the terminating load impedance, the action of the output matching network, and the device equivalent output impedance determined from the Rieke diagram are shown in regard to the general circuit design problem.

6. Arguments against the existence of a conjugate match in combination with the desired operating impedance contours as determined by the Rieke diagram data. Further insistence that max. gain and max. efficiency as a power amplifier do not result from the same contours.

7. Efficiency of power amplifiers under various operating conditions is highlighted as a function of drive and overdrive. Effects of various drive levels on actual device conjugate power load impedances is examined from a circuit design and efficiency perspective.

8. Wrapped up section 3 with further complications from adding in more equivalent circuit elements and real devices. Effects of feedback, load impedance , source impedance, and decoupling networks are briefly and lightly touched upon. Definition of conjugate match in terms of S-parameters is relied upon to show conditions of existence.

9. Gain of a power or low noise amplifier is discussed with respect to the developed impedance contours for maximum power output, maximum efficiency, best linearity, or low noise. The gain is shown to depend on the impedance contours so developed and the mis-match from these contours compared to the ideal contours derived from the ideal equivalent circuit of the device.

The gain of any amplifier can be shown to be due to three factors:

1. The gain or loss of the input matching circuit.

2. The device transducer gain (|S21|)**2.

3. The gain or loss of the output matching circuit.

These considerations are completely general and may include active circuits such as followers etc. It is useful to recall that passive LC networks cannot exhibit gain per se but do present minimum loss when terminated with the conjugates of the desired image impedances on each end. This parameter may then be referred to as the available gain of the network. Any additional loss, Lm, above this number is strictly due to mis-match characterized as follows:

Lm = 1/(1-|S11|)**2

S11 is the reflection coefficient with the other port of the network terminated in the conjugate of its input impedance.

Loss of the output matching network is computed the same way except |S22| replaces |S11| in the above expression. The frequency dependence of the networks can be seen by inserting different values of |S11| and |S22| over the bands of interest. If this is done, the absolute minimum value of loss through the passive networks occurs when both are matched to the conjugates of their image impedances. More complex networks involving active or passive elements may be characterized in the same way. Note that the expression for Lm simply accounts for that portion of voltage reflected from the opposite end of the network. The squared term is necessary to compensate for the fact that the normalized incident wave was defined as 1/Vi**1/2. If a two-port passive network used as an impedance matching network is connected to both ports of a VNA, it will in all probability appear lossy unless having been designed for 50 Ohm input and output impedances. The min. loss computation can then be computed by hand or by computerized circuit analysis methods. Controlled input mis-matches can be used to stabilize gain over a given band to a fixed number.

The associated gain parameter, mentioned in Sec. 3, can now be seen to be a sum of
Lm in + |S21|**2 + Lm out.
But, the associated gain is still dependent on, for a given performance specification, the mis-match seen from the device input/output terminals. Again, we reiterate that the max. gain from the device is obtained when the apparent input/output port impedances are approached by conjugates of the device parallel RC equivalents. However, the S-parameter techniques discussed here can only be fully applied to passive networks and linear small-signal devices. These techniques cannot be fully applied to large-signal (power) amplifiers. For these we can only use the S-parameters to analyze the passive elements and our load-pull/source-pull data.

There is a joker in the deck, however. Feedback can be applied to modify device impedances at either the input or the output or both. For example, feedback around the common op-amp in the inverting configuration (voltage shunt feedback or trans resistance) forces Zi -> 0 Ohms while Zo -> higher. Three other varieties of feedback are possible to modify the input/output impedance of a given stage. But, feedback is only useful while the stage stays linear or close to it AND there is sufficient gain to afford some loss of gain through feedback. My own experiments with active RF feedback at -- showed that RF feedback DID NOT control the RF amplifier stage once it approached

compression and, of course, efficiency and output power also tanked. Feedback can be unintentional due to lead inductance and resistance as well as |S12| (the Reverse Transmission) through the device.

Neutralization seeks to minimize |S12| over a narrow band of frequencies or at one spot frequency while the much harder process of Unilateralization seeks to force |S12| -> 0 over all frequencies and not just those of interest. Unintentional feedback can be caused by improper grounding techniques or series resistances in the leads of the device-particularly at the cathode/emitter/Source lead in common cathode/emitter/Source topology amplifiers. [I am assured that failure to swiftly bring the grid/base/gate to ground is just as lethal to stability in grounded grid/base/gate designs.] Many an RF designer has tried to use the marvelous little 50 Ohm MMIC gain blocks-usually consisting of a shunt-series feedback Darlington pair of silicon transistors or HBTs-only to find gain obtained is not as advertised. All seems lost until some old *RF Salt* advises the user about their grounding technique not being adequate enough for the frequencies of interest. I have also conjectured that, in my research, some feedback through |S12| may be tolerated IF no stability penalties ensue and it results in reflections that are helpful in modifying the input or output device port impedances. I do note that this primarily affects one side or the other. Analytical tools of the sort discussed here in conjunction with Cripps' method are sufficient for approximation in design but cannot get all the way there for non-linear applications.

Stability has not been discussed in this work except in the abstract or lack thereof. Means to insure stability defined here as insensitivity to input/output terminations usually take two forms. The device is either unconditionally stable or can be made so by giving up some gain at the "troublesome" frequencies or within the desired band through the use of "stoppers", beads, swamping, etc. Or the device is marginally stable and the input/output impedance ranges must be restricted either by circuit design using methods such as those above or the use of circulators/isolators or hybrids, where practical. In general, stability can be assured when the stray coupling is -10 to -15 dB below |S12| for a given stage and well below the total gain for an amplifier. The maximum stable gain of any stage may be estimated as :

MSG = |S21|/|S12| where these are scalars or
MSG = |S21| - |S12| where these are logs [dB]

Note that other types of oscillations can occur as the device Ft is approached since ANG S12 deviates away from 180 degrees (for common cathode/emitter/Source topology amplifiers) at high frequencies. This effect can be easily seen in differential or push-pull amplifiers.

Summary

We started off considering that a power amplifier was defined as a device operating at maximum voltage and current nearly in phase such that maximum power can be delivered to the load. If the amplifier is operating in a linear, non-saturated, non-

switching mode such as class A, AB, or B or any of their derivatives, then the device will conduct over a number of degrees of the input wave. This number will range between 360 degrees and something less than 180 degrees of the input wave. In any given device, there is an optimum load impedance such that the voltage and current delivered to the load is a maximum while the device dissipation is minimized or, put another way, the efficiency is optimized.

The impedance that offers maximum power output and maximum efficiency can be measured using Load-Pull and Source-Pull techniques. An approximate equivalent circuit of the intrinsic low frequency device can be generated from RC parallel circuits which does not have the complications of inter electrode capacitances, lead inductances, and so on. These effects are easily accounted for by the use of Miller's theorems for Linear, small-signal analysis. The RC parallel circuits that represent the device equivalent impedance were seen as dissipative physical networks not as some authors have alleged, fictitious.

The definitions of both conjugate match and maximum available device gain were examined from many viewpoints where it was concluded that the device is conjugate matched when delivering maximum available gain NOT power. The optimum load-line for all devices was seen as radically different in most cases from that providing maximum gain. For all kinds of devices, the internal parasitics were determined to a first order to either be above or below the desired load-line impedances for maximum power or best efficiency at the output and therefore may or may not require absorption by tuning.

Using S-parameter notation, the conjugate match was rigorously defined for multi-port networks. At the same time, the procedure for obtaining the impedance contours for any device operated at maximum power and/or efficiency was outlined but little commonality was found between the two and very little commonality seems to be observed in practice.

It cannot be stressed enough that all "Load-Line" approximations are just that, approximations that become increasingly inaccurate as the device operating conditions depart from Class A. The Load-Line is also known to broaden into a load ellipse when presented with reactive loads such as off-frequency tuned circuits. So, even in the class A case, the RF output circuit parameters can be challenging to calculate in the time domain. Away from Class A, the voltage and current swings are such that the "Load-Line" concept is an artifice and not a very helpful one at that. It is much more useful and intuitive to speak of the voltage and current trajectories traversed within the device characteristics. It is fortunate, perhaps, that most microwave devices at high frequencies operate at Class A to extract the extra 5-6 dB gain from them that would otherwise be surrendered in Class B. The examination of the trajectories shows that Class B is indeed something of a special case or inflection point in that the tuned circuit load now has equal or greater effects on the output wave shape than the active device. However, no analytical support could be found for the notion by some authors that, in Class B, a conjugate match is guaranteed by these conditions. The only support for such a contention exists in cases of extreme overdrive or under drive as commented by other critics of the various papers presented on the topic.

Obviously there are many misconceptions about amplifier circuits and RF amplifiers in particular. By examining the behavior of amplifiers at low frequencies we were able to deduce the forms of the equivalent circuits without getting overly complex. The point has been made that a Class A FET or vacuum tube does not absorb power from its driving source until operated at a sufficiently high frequency where transit time delays cause a shunting admittance to appear at the input.
The Miller admittance can be somewhat modified by the external environment but is largely dependent on device construction and dimensions. The above caveats do not apply to bipolar transistors (BJTs) die to their current driven action though the same shunting effects occur as well as distributed effects unique to bipolars. Although the equivalent circuit approach was shown to be only analytically satisfied for small-signal conditions, it has nonetheless provided a starting point which turns out to be close enough for some conclusions to be drawn.

The conjugate match, as it exists within the available amateur literature and using the formal notations of circuit theory, was shown to be somewhat at odds. The conjugate match, as referred to in the literature consulted referred to zero reflections between the device output impedance and the device output matching network for maximum power and or efficiency. Circuit design literature defines conjugate matching as that match existing between the output of the device and the output matching network that results in zero reflections with maximum GAIN. In almost all cases, these two cannot co-exist with the same networks except perhaps at far microwave where any power you might obtain occurs at maximum gain by default. Neither overdrive, under drive, nor classes of operation will change the basic incompatibilities between these two definitions. Thus, I am forced to conclude, someone got it very wrong early on and observed a fortuitous coincidence of tuning, class of operation, and gain that resulted in zero reflections but this is not borne out by theory or practice except in very special cases. The conjugate match does not exist as defined in the amateur literature nor should it be expected to exist. The only thing that matters is obtaining and attaining in any given circuit design the correct conjugate impedance contours at input and output for the frequencies of interest to achieve maximum power or efficiency.

Operation in classes other than Class A complicate matters as it has been shown that the analytical tools available to us deteriorate significantly in utility. Any apparent "slop" in calculations is likely to be found there as the concepts are extended beyond reasonable analytical realms of applicability. It is the author's contention that examining the issues from a broader perspective of both tube and solid state design as experienced and practiced by him has allowed the development of new insights into what has been going on which he hopes has been adequately conveyed. Within the discipline of solid state, MIC, and MMIC design, the conjugate match and load-line problems become clear and distinct although the physical interpretations and realizations of functional circuits may not be.

Notes:

1. My lovely spouse wrote an integral which is piecewise continuous covering this relationship in a design report she did at -- . I later found that someone had already done this but it is the thought and the understanding that count.

2. The first tube in production not to exhibit this problem up to 20-30 MHz or so was the 6AC7 and was later improved by the 6AG7 for those who could burn current. Earlier pentodes like 6D6 etc. show reduced sensitivity even at 14 MHz owing to the grid admittance. The effect can be "somewhat" ameliorated by slight cathode inductance but watch out-these can also be known as "oscillators". Keep those grounding leads short!

3. There are other less polite terms for it when doing many frequencies over many bias conditions.